AMENDMENTS TO THE SPECIFICATION:

Insert the following paragraph after the paragraph ending on page 6, line 21:

In the frame sync detector, there are at least one I-sync processor and at least one Q-sync processor. As shown in Fig. 2, the I-sync processor includes a first I-binary adder 22; an I-memory device 23, the I-memory device 23 coupled to the first I-binary adder; a reference sync 26; an I-multiplier 25, wherein the I-multiplier multiplies the reference sync 26 with the output of the I-memory device 23; an I-accumulator, wherein the I accumulator comprises: a first I-register bank 27; a second I-adder 28, the second I-adder 28 having at least two inputs, wherein one of the two inputs is coupled to an output of the first I-register bank 27; a second I-register bank 29, wherein an output of the second I-register bank 29 is coupled to an input of the second I-adder 28; and an I-squaring device 29. The Q-sync processor includes a first Q-binary adder 22A, a Q-memory device 23A, the second Q-memory device 23A coupled to the first Q-binary adder 22A; a reference sync 26, a Q-multiplier 25A, where in the Q-multiplier 25A multiplies the reference sync 26 with the output of the Q-memory device 23A; a Q-accumulator, wherein the Q-accumulator comprises a first Q-register bank 27A; a second Q-adder 28A, the second Q-adder 28A having at least two inputs, wherein one of the two inputs is coupled to an output of the first Q-register bank 27A; a second Q-register bank 29A, wherein an output of the second Q-register bank 29A is coupled to an input of the second Q-adder 28A; and a Q-squaring device 29A.